A Memorandum

**To:** Nuri Emanetoglu, Associate Professor / Andrew Sheaff, Lecturer

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**Date:** October 3, 2018

**Subject:** Part Order 2 Justification

Due to readability the schematic corresponding to this memorandum is contained within the Dufour/Robb senior project Google Drive folder. It is named “PO2 Justification Schematic.pdf”, we apologize for this inconvenience, but attempts to include the image here failed to produce a readable image.

The STM32L476 64-pin LQFP is the selected microcontroller due to not only it’s familiarity with the project team, but because of the CMSIS libraries which contain various DSP functions that are useful in dealing with fast fourier transforms. The 64 pin package is identical to the chip used on the STM32L476 Discovery Board, which is being used for prototyping purposes on this project. The MCU features a 12-bit SAR ADC. The ADC resolution has been found through Matlab simulations to be sufficient for capturing the input signal. In addition the ADC is capable of sampling at 10ksps which has been found experimentally to be adequate for capturing the fundamental periodicity of input frequency range. The code used for prototyping would be able to be ported over the the new chip with minimal alterations. In addition, this model features the necessary program memory available to handle to the overhead required by the CMSIS DSP libraries. In addition, ample RAM is required in order to handle the minimal buffer size of data points necessary to capture the slowest signal present in the project specifications (60Hz). This buffer size has currently been calculated to be 1024 samples. These samples will be single precision floating point numbers and several temporary buffers will be required to perform the peak detection algorithm.

The chip requires three 10 kOhm pull-down resistors, these serve to pull down the floating outputs of the JTAG/SW interface that will be used to debug and program the MCU. In addition, the MCU requires several decoupling capacitors. One 100nF is recommended for each Vdd pin on the MCU. A 4.7uF tantalum capacitor is also recommended; the tantalum capacitor composition are more stable at higher frequencies than that of ceramic capacitors. The tantalum features a high ESR which is what it is positioned in parallel with the ceramic capacitors which feature a much lower ESR.

Female jumpers have been chosen as a way of selecting the boot state of the MCU. The boot configuration can be changed by setting the BOOT0 pin to either a logic 0 or logic 1. The jumper allows for this selection to be changed on the fly depending on which configuration is needed.

The push button is needed to reset the device and is recommended by the official STM design manuals as way increasing usability and as well as forcing a reset in case of device malfunction. The off-momentary-on topology was chosen as the button should be pushed once for a reset and does not need to stay in an “on” state to serve its purpose.

The ABL2 external crystal oscillator is a necessary component for the circuit as there are many factors that affect the STM32L476 64-pin LQFP microcontroller. The internal oscillator of the STM32L476 64-pin LQFP can only be calibrated to within 3% of the specified frequency according to the datasheet. The external crystal oscillator, ABL2, is within 30 ppm (parts per million), which equates to .003% of the specified frequency.

The 0603 X5R 2.2uF 16V capacitors were selected in order for the LDO to operate. The input 2.2uF capacitor serves to minimize input ripple similar to the mirrored 2.2uF output capacitor. The 10nF capacitor tying the soft-start line to ground is how the the start up time of the device is configured. The initial output voltage is limited by the capacitor in order to provide a smoother ramp to the output voltage.

The Analog LDO regulator (ADP1714), 3V3 output, 300mA, is needed to drop the voltage down from the 5V source from the analog side of the circuit. The STM32L476 chip being used requires 3.3V to operate and thus can not work with buck converter supply being used for the analog circuitry. Another problem posed by the buck-converter topology is that since it is a switch-mode-power-supply it features high frequency content in its output voltage. This high frequency can cause issues with the STM32L4 operation. Therefore, a LDO is prefered due to outputting a nearly DC voltage with very minimal ripple. A ferrite bead is recommended to provide external filtering from the Vdd to Vdda rails. It is recommended to use external filtering to separate these two pins. This is important for this project because Vdda is the supply pin for the ADC and noise on this line can manifest as conversion errors. Vdda is tied to the Vref pin of ADC internally on the 64-pin package.

The 20pF capacitors were calculated by using the formula corresponding to the Pierce Oscillator topology, CL = (C1\*C2)/(C1+C2)+Cstray. This will give accurate and stable results out of the crystal.The load capacitance given by digikey is 18pF for the 8MHz HSE crystal oscillator. The stray capacitance is rated at 7pF, so design considerations will account for this. Any capacitor value of 20pF to 22pF will work for this purpose. The CAP CER 20PF 50V NPO 0603 is sufficient for this purpose.